

Update Search

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	24557	((pe) (plasma adj enhanced)) adj2 (cvd (chemical adj vapor adj deposit\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/22 14:51
L3	6376	2 same ("Si.sub.3N.sub.4" (silicon adj nitride))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/22 15:02
L4	269	3 and ((low near5 frequenc\$3) same (high near5 frequenc\$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/22 15:36
L5	10875	spacer\$1 with ("Si.sub.3N.sub.4" (silicon adj nitride))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/22 15:36
L6	26	4 and 5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/22 15:36
L7	25892	gate\$1 with ("Si.sub.3N.sub.4" (silicon adj nitride))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/22 15:36
L8	46	4 and 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/22 15:36

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L10	9860	((pe) (plasma adj enhanced)) adj2 (cvd (chemical adj vapor adj deposit\$4))	US-PGPUB	OR	OFF	2006/11/22 15:46
L11	2676	10 same ("Si.sub.3N.sub.4" (silicon adj nitride))	US-PGPUB	OR	OFF	2006/11/22 15:46
L12	23	11 same ((low near5 frequenc\$3) same (high near5 frequenc\$3))	US-PGPUB	OR	OFF	2006/11/22 15:47
L13	1	12 same spacer\$1 same gate\$1	US-PGPUB	OR	OFF	2006/11/22 15:48
L14	4	12.clm.	US-PGPUB	OR	OFF	2006/11/22 15:48

Day : Wednesday
Date: 11/22/2006
Time: 15:52:02



Inventor Name Search Result

Your Search was:

Last Name = RAMACHANDRAN

First Name = RAVI

Application#	Patent#	Status	Date Filed	Title	Inventor Name
07369475	4937541	250	06/21/1989	LOADED LANGE COUPLER	RAMACHANDRAN, RAVI
07551426	5051705	150	07/10/1990	GAIN-TILT AMPLIFIER	RAMACHANDRAN, RAVI
07588766	5066926	150	09/26/1990	SEGMENTED CASCODE HBT FOR MICROWAVE-FREQUENCY POWER AMPLIFIERS	RAMACHANDRAN, RAVI
08359539	5657326	150	12/20/1994	RADIO BASED COLLISION DETECTION FOR WIRELESS COMMUNICATION SYSTEM	RAMACHANDRAN, RAVI
09022069	6751272	150	02/11/1998	DYNAMIC ADJUSTMENT TO PRESERVE SIGNAL-TO-NOISE RATIO IN A QUADRATURE DETECTOR SYSTEM	RAMACHANDRAN, RAVI
09207781	6662135	150	12/09/1998	METHOD AND APPARATUS FOR REFLECTIVE MIXER TESTING OF A CABLE MODEM	RAMACHANDRAN, RAVI
10256297	6884754	150	09/27/2002	AQUEOUS COMPOSITIONS FOR SEED TREATMENT	RAMACHANDRAN, RAVI
10256323	Not Issued	161	09/27/2002	Aqueous neonicotinoid compositions for seed treatment	RAMACHANDRAN, RAVI
10259498	Not Issued	71	09/30/2002	Offline learning synchronization system	RAMACHANDRAN, RAVI
10919626	Not Issued	71	08/17/2004	AQUEOUS NEONICOTINOID COMPOSITIONS FOR SEED TREATMENT	RAMACHANDRAN, RAVI
11069021	Not Issued	93	02/28/2005	AQUEOUS COMPOSITIONS FOR SEED TREATMENT	RAMACHANDRAN, RAVI
60325829	Not Issued	159	09/28/2001	Aqueous compositions for seed treatment	RAMACHANDRAN, RAVI
60325902	Not Issued	159	09/28/2001	Aqueous neonicotinoid compositions for seed treatment	RAMACHANDRAN, RAVI
60454723	Not Issued	159	03/17/2003	Various vascular closure devices	RAMACHANDRAN, RAVI
60575076	Not Issued	159	05/27/2004	Biomarkers for monitoring IMPDH pathway inhibition	RAMACHANDRAN, RAVI

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**PALM INTRANET****Inventor Name Search Result**

Your Search was:

Last Name = KELLIHER

First Name = JAMES

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10710257	Not Issued	71	06/29/2004	METHOD OF FORMING SIDEWALL SPACER USING DUAL-FREQUENCY PLASMA ENHANCED CVD	KELLIHER, JAMES T.
10905588	Not Issued	71	01/12/2005	OXYGEN BARRIER LINER IN A LOW-K CAP LAYER	KELLIHER, JAMES T.
11164419	Not Issued	30	11/22/2005	OPTIMIZED SiCN CAPPING LAYER	KELLIHER, JAMES T.

Inventor Search Completed: No Records to Display.

Search Another: Inventor

Last Name	First Name	
<input type="text" value="kelliher"/>	<input type="text" value="james"/>	<input type="button" value="Search"/>

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PALM INTRANET

Day : Wednesday
Date: 11/22/2006
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Inventor Name Search Result

Your Search was:

Last Name = NARASIMHA

First Name = SHREESH

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>10249295</u>	Not Issued	61	03/28/2003	CMOS DEVICE INTEGRATION FOR LOW EXTERNAL RESISTANCE	NARASIMHA, SHREESH
<u>10250241</u>	Not Issued	41	06/17/2003	High-performance CMOS devices on hybrid crystal oriented substrates	NARASIMHA, SHREESH
<u>10314023</u>	Not Issued	161	12/05/2002	Method and structure for reduction of junction capacitance in a semiconductor device and formation of a uniformly lowered threshold voltage device	NARASIMHA, SHREESH
<u>10605311</u>	6991979	150	09/22/2003	METHOD FOR AVOIDING OXIDE UNDERCUT DURING PRE-SILICIDE CLEAN FOR THIN SPACER FETS	NARASIMHA, SHREESH
<u>10664714</u>	6825102	150	09/18/2003	METHOD OF IMPROVING THE QUALITY OF DEFECTIVE SEMICONDUCTOR MATERIAL	NARASIMHA, SHREESH
<u>10710001</u>	7071072	150	06/11/2004	FORMING SHALLOW TRENCH ISOLATION WITHOUT THE USE OF CMP	NARASIMHA, SHREESH
<u>10710257</u>	Not Issued	71	06/29/2004	METHOD OF FORMING SIDEWALL SPACER USING DUAL-FREQUENCY PLASMA ENHANCED CVD	NARASIMHA, SHREESH
<u>10763308</u>	Not Issued	93	01/23/2004	CMOS DEVICE INTEGRATION FOR LOW EXTERNAL RESISTANCE	NARASIMHA, SHREESH
<u>10835949</u>	7001844	150	04/30/2004	MATERIAL FOR CONTACT ETCH LAYER TO ENHANCE DEVICE PERFORMANCE	NARASIMHA, SHREESH
<u>10905024</u>	Not Issued	41	12/10/2004	DEVICE HAVING DUAL ETCH STOP LINER AND PROTECTIVE LAYER AND RELATED METHODS	NARASIMHA, SHREESH
<u>10905025</u>	Not Issued	41	12/10/2004	DEVICE HAVING ENHANCED STRESS STATE AND RELATED METHODS	NARASIMHA, SHREESH
<u>10905027</u>	Not Issued	71	12/10/2004	DEVICE HAVING DUAL ETCH STOP LINER AND REFORMED SILICIDE LAYER AND RELATED METHODS	NARASIMHA, SHREESH
<u>10906366</u>	Not Issued	41	02/16/2005	STRUCTURE AND METHOD FOR IMPROVED DIODE IDEALITY	NARASIMHA, SHREESH